IEEE University of Toronto Student Branch - ASIC Team

The ASIC Team is a new initiative started by undergrads in the IEEE Student Branch to introduce practical IC design and tapeout opportunities to the undergrad class. This document will introduce the team's objectives, technical stack, and more!

Mission Statements

1. Creating practical IC Design Opportunities for Students.
2. Contributing back to the Open Source Silicon Community.
3. Creating Resources for interested parties in IC design.

Activities

Core Tapeout

Throughout the year, members of the team participate in learning sessions where they get familiar with open source IC toolchains. Using this knowledge each member prototypes their own proposed design, this is our *ASIC Kompetition*. The winning designs are based on an internal vote. Once chosen, the entire team comes together to tapeout these chips through TinyTapeout.

Workshops

The ASIC Team also has workshops and paper reviews slated, these technical sessions are open to the broader student body. Team members have put forward workshop plans such as: *An Introduction to Asynchronous Circuits* and *An Introduction to AI-Assisted EDA*. Catching students up with the SoTA in ICs.

Community Building

The purpose of the ASIC team is to build a passionate community of IC designers at the University of Toronto. To facilitate this, we run events like the IC job mixer, an event open to all students introducing them to the ASIC design flow and what different careers fit in this workflow.

About the Team

We have a vast team of 18 engineering undergrads joining our team as associates, with 2 directors leading the show. Our events have a tremendous impact, with our community events reaching 60+ students in attendance, and over 100 students applied to even join the team. We are thrilled that the passion for ICs and electronics continues to grow stronger at UofT.

Previous Projects

This is now the second year of the ASIC team, the first was a small trial run to build the grassroots. The product of our first year was a DPLL project, which is slated to be taped out on the TT-Sky-25b shuttle.

Technical Stack

Due to the limited availability and high cost of proprietary IC design software traditionally used, the team has adopted an open source tech stack, utilizing the resources and tools from the amazing FOSSi community to build opportunities for students. While limited, we ensure our members contribute to every phase of the IC design workflow.

Process Node: SKY130
Toolchain Flow: LibreLane
Tooling: Open Circuit Design
Tapeout Provider: TinyTapeout

Want to Help?

If you're as interested as we are about bringing practical experience and building a community of silicon engineers at UofT, we would love your help in enabling this! We appreciate any and all assistance, in whatever form it takes from the larger professional community around the world. Below are a few examples of ways you can help out.

Mentorship

Mentorship and participating in our design reviews are immensely helpful for our associates. Your mentorship will bolster our learning experience, grow the professional network of our engineers-in-training, and provide priceless feedback to our team.

Services & Products

What little liquid cash we have is often spent purchasing tapeouts, prototyping equipment or services. If your organization can provide some of these to our team it would free up a lot more budget to tapeout and grow our community building events.

Monetary

We project around a $750CAD cost per tapeout; As we get more money, we can provide more tapeout opportunities to our associates. Monetary contributions would greatly benefit the team's ability to target our mission statements and scale the team.

Get in Touch

Please don't hesitate to reach out to us with questions or inquiries, you can email our team at projects@ieee.utoronto.ca