Click ~Clock

Designing Asynchronous Circuits

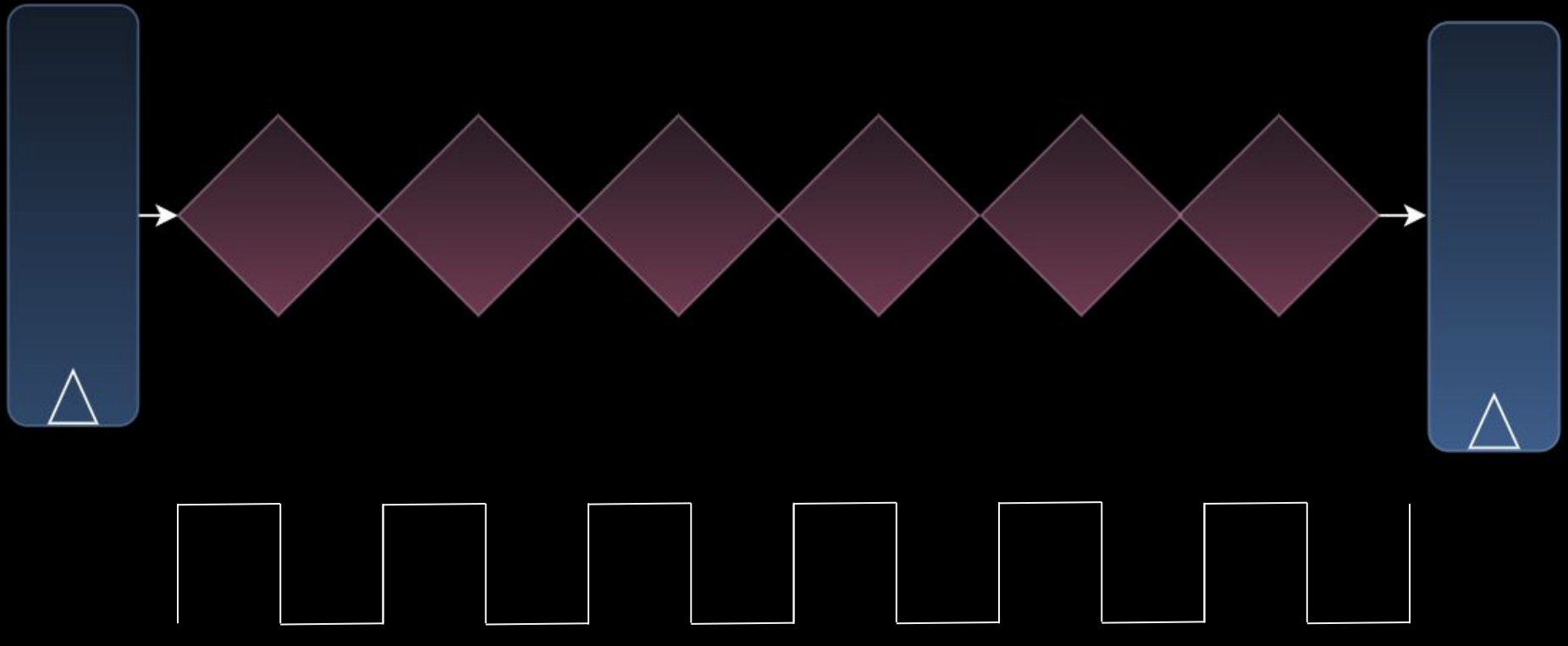
10 / 08

Presented by

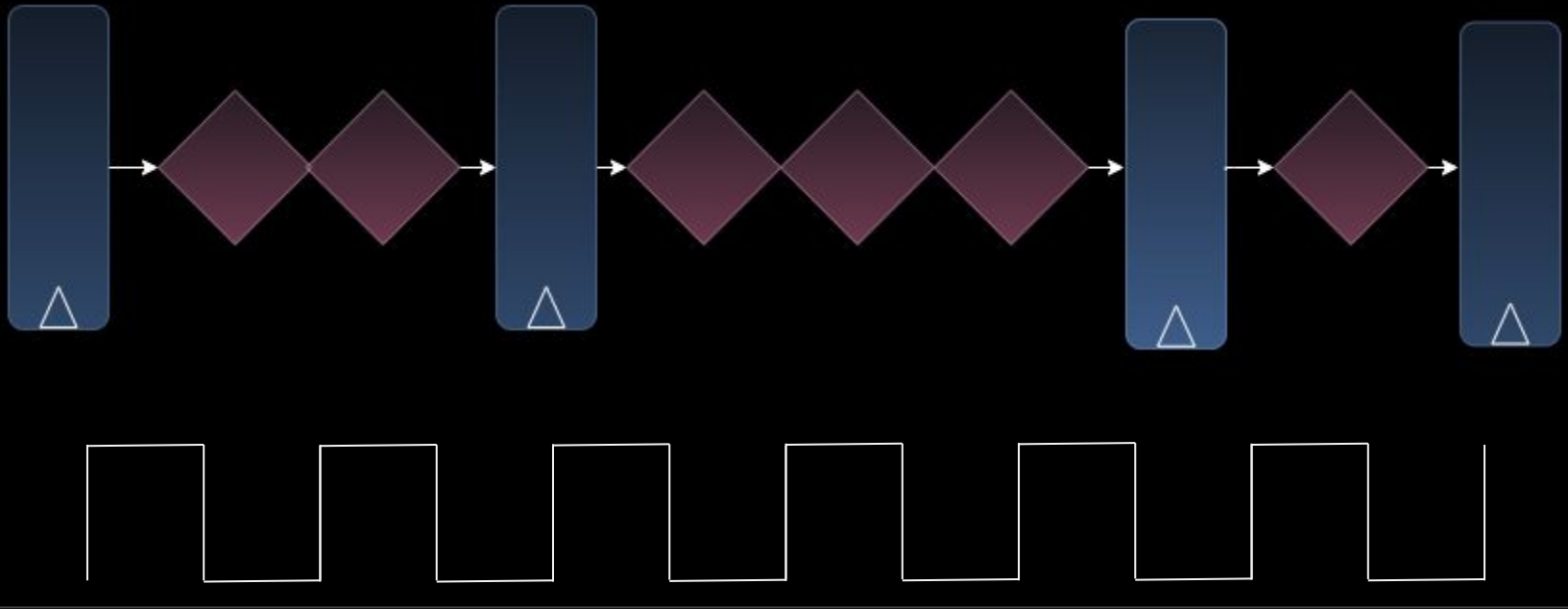
Vishwa Eswaran

UNIVERSITY OF TORONTO
IEEE STUDENT BRANCH

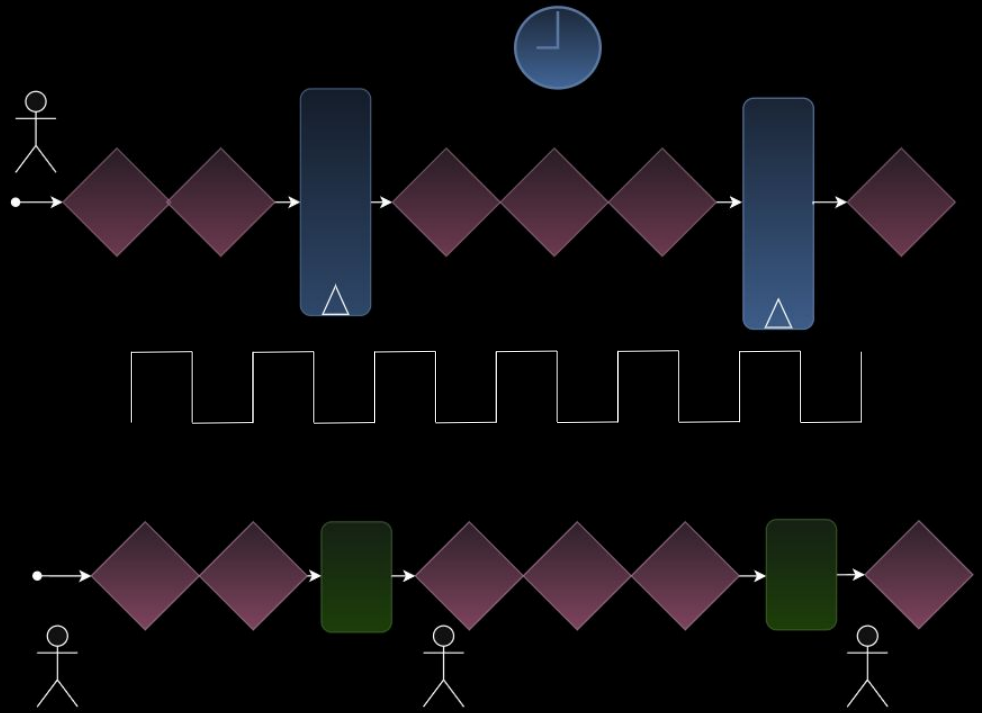
Classic Pipelining



Classic Pipelining



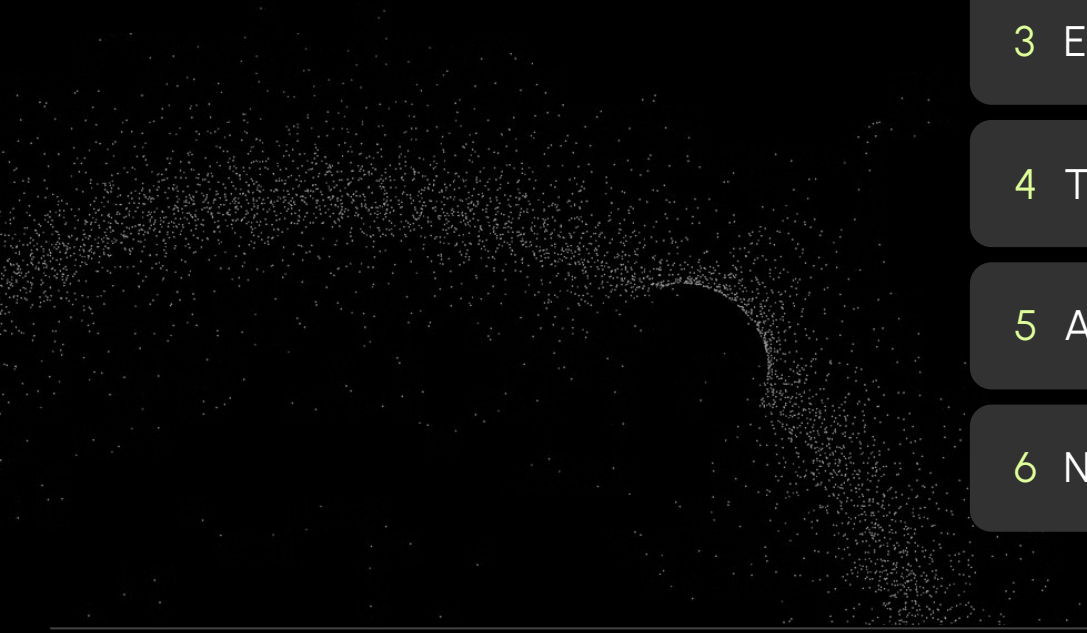
Two Pipelines



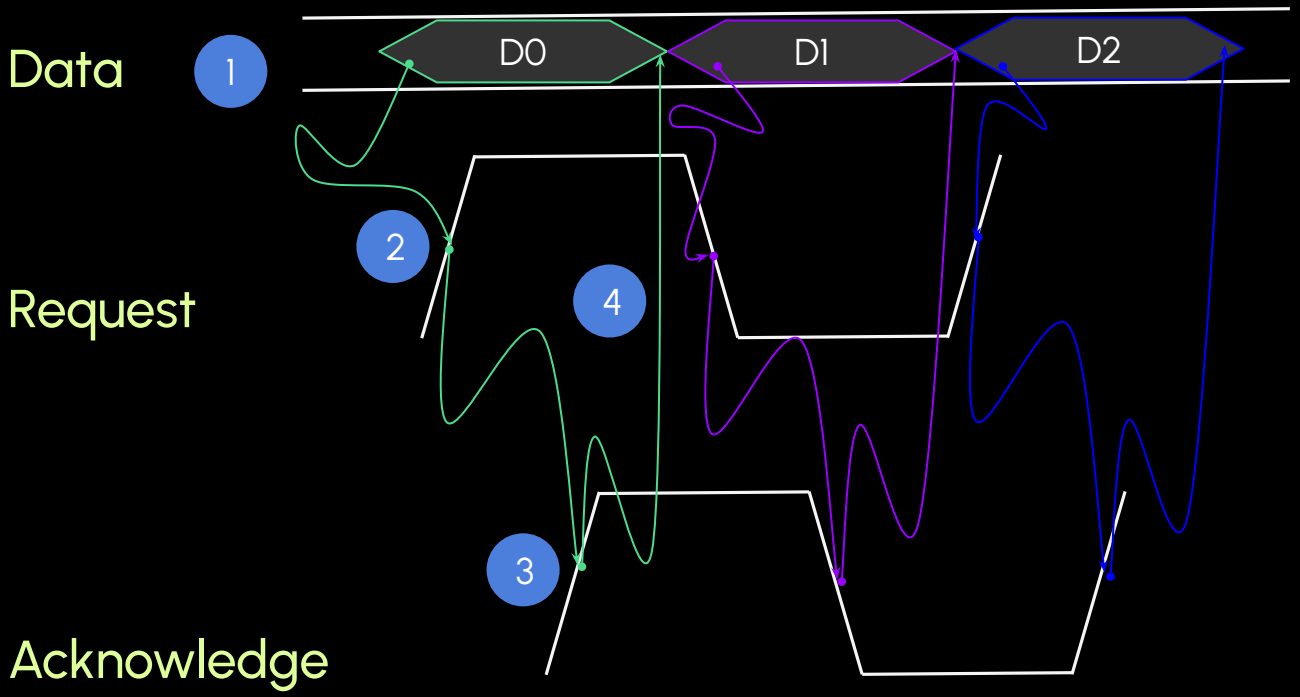
In Asynchronous Pipelines

Average worst case delay reduces.

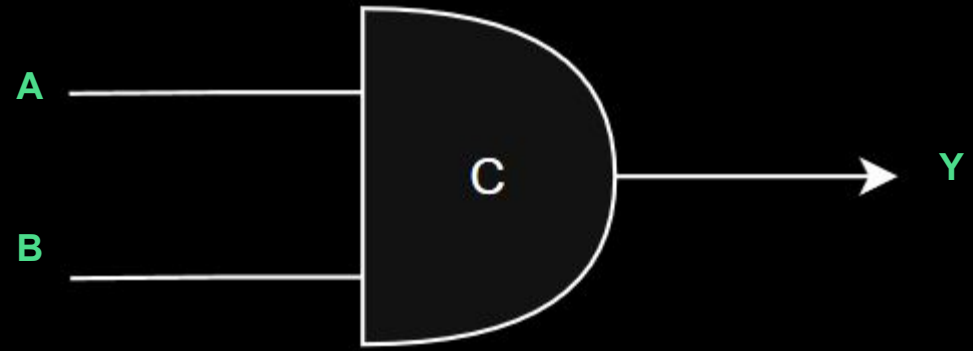
World of Asynchronous Circuits



Two Phase Communication



Muller C Element

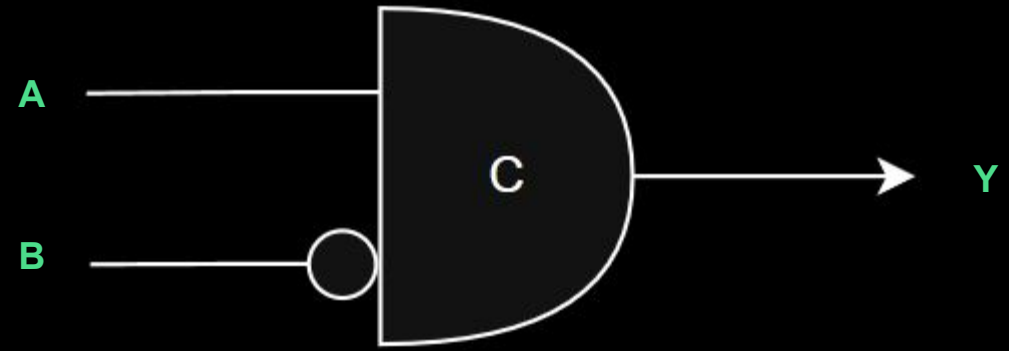


Muller C Element

0 - 😐
1 - 😃

A	B	Y
😐	😐	0
😐	😃	Y
😃	😐	Y
😃	😃	1

Muller C Element

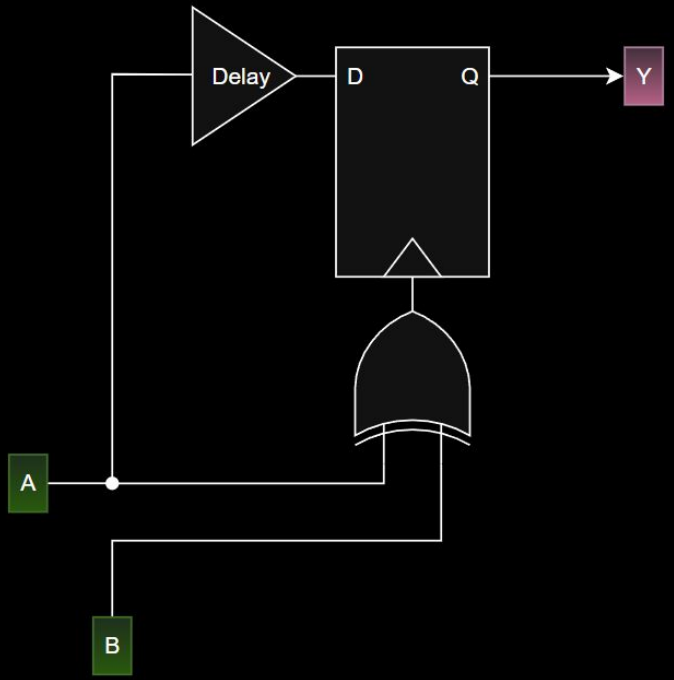


Muller C Element

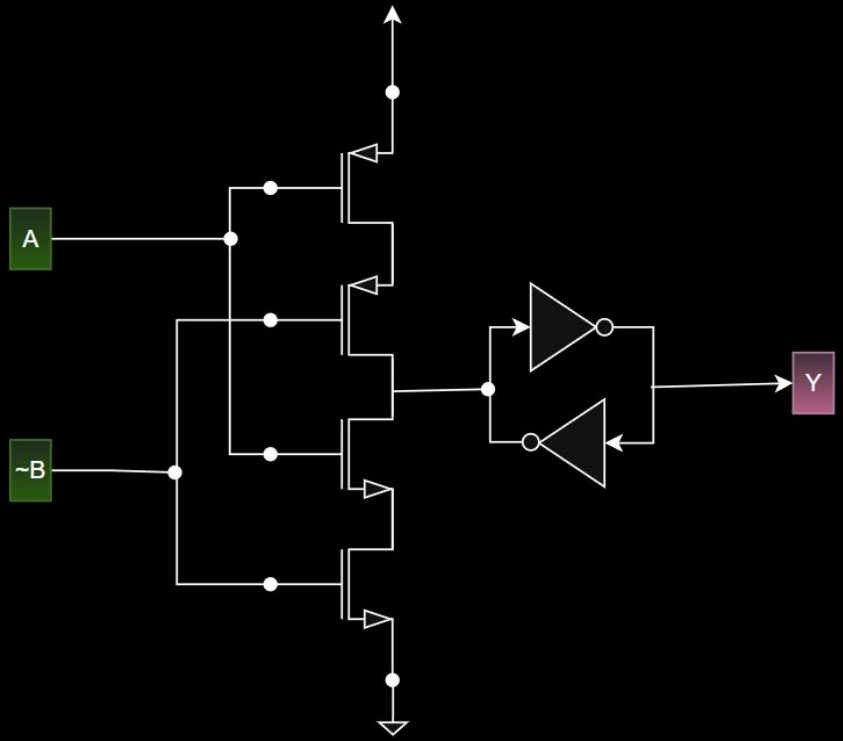
0 - 😐
1 - 😃

A	B	Y
😐	😐	Y
😐	😃	0
😃	😐	1
😃	😃	Y

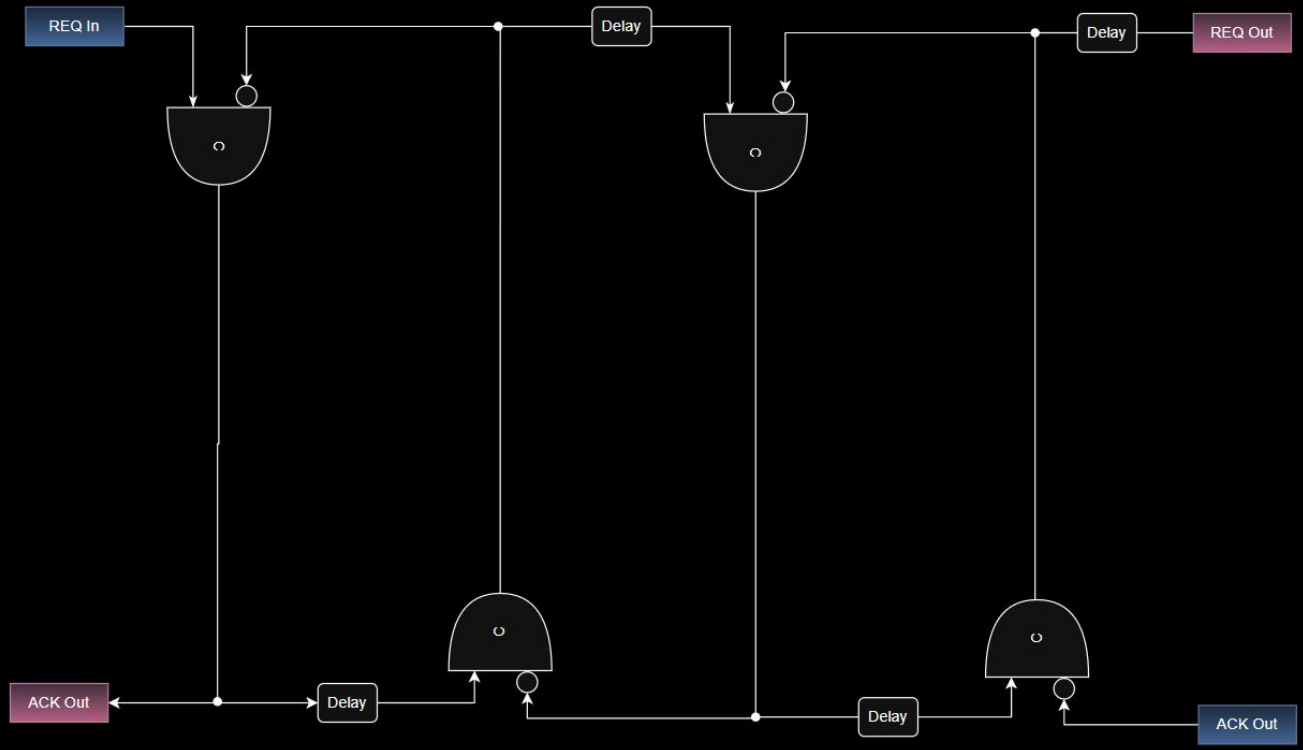
Muller C Element



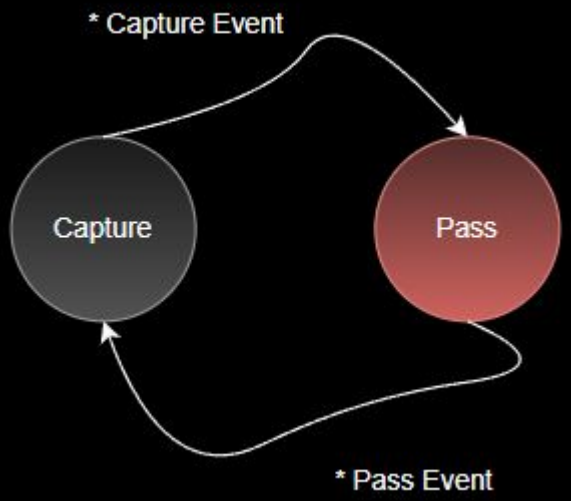
Muller C Element



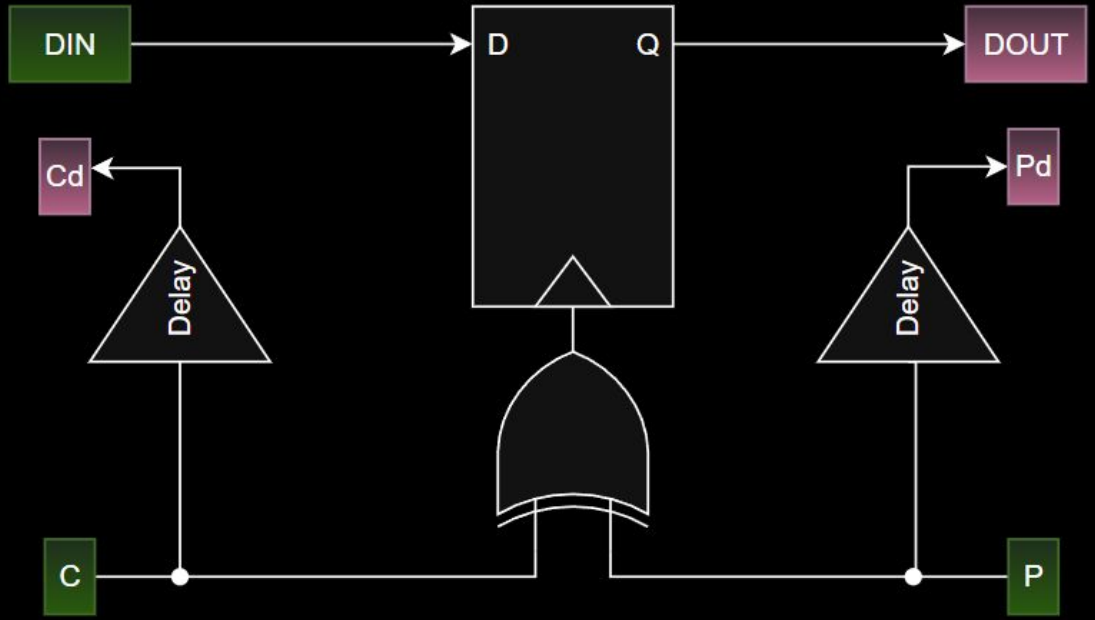
Control Path



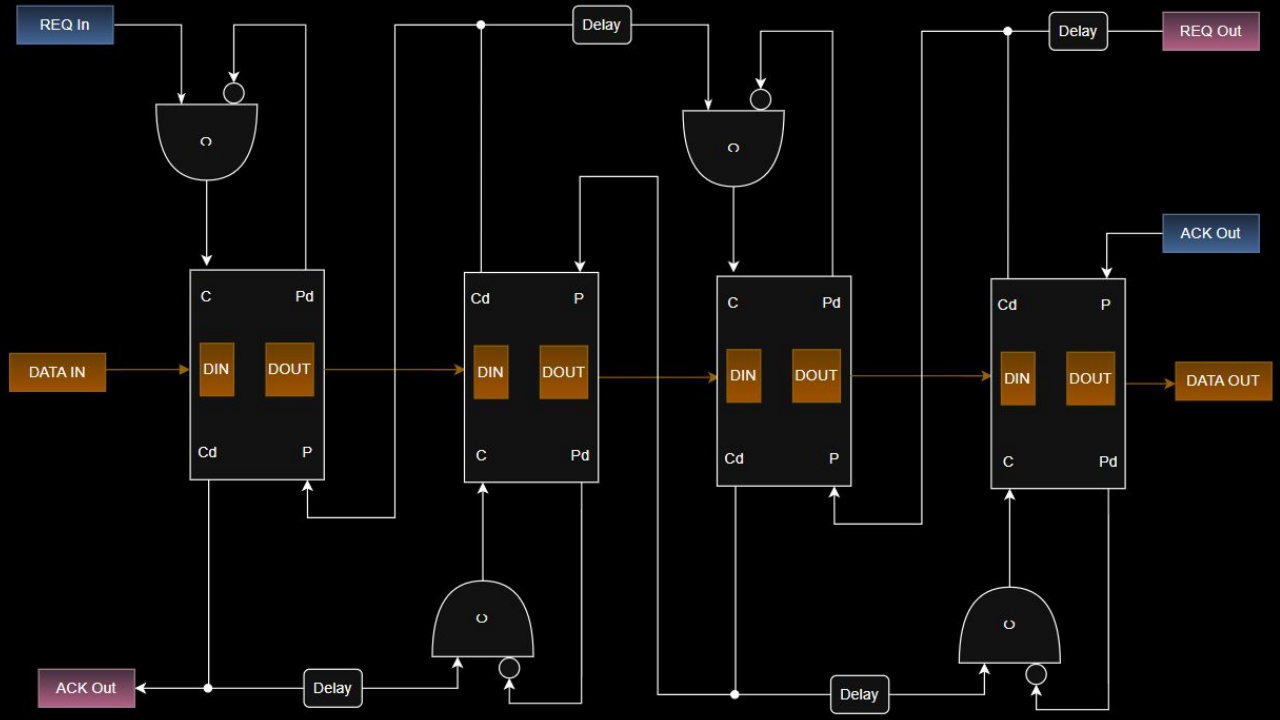
Event Driven Register



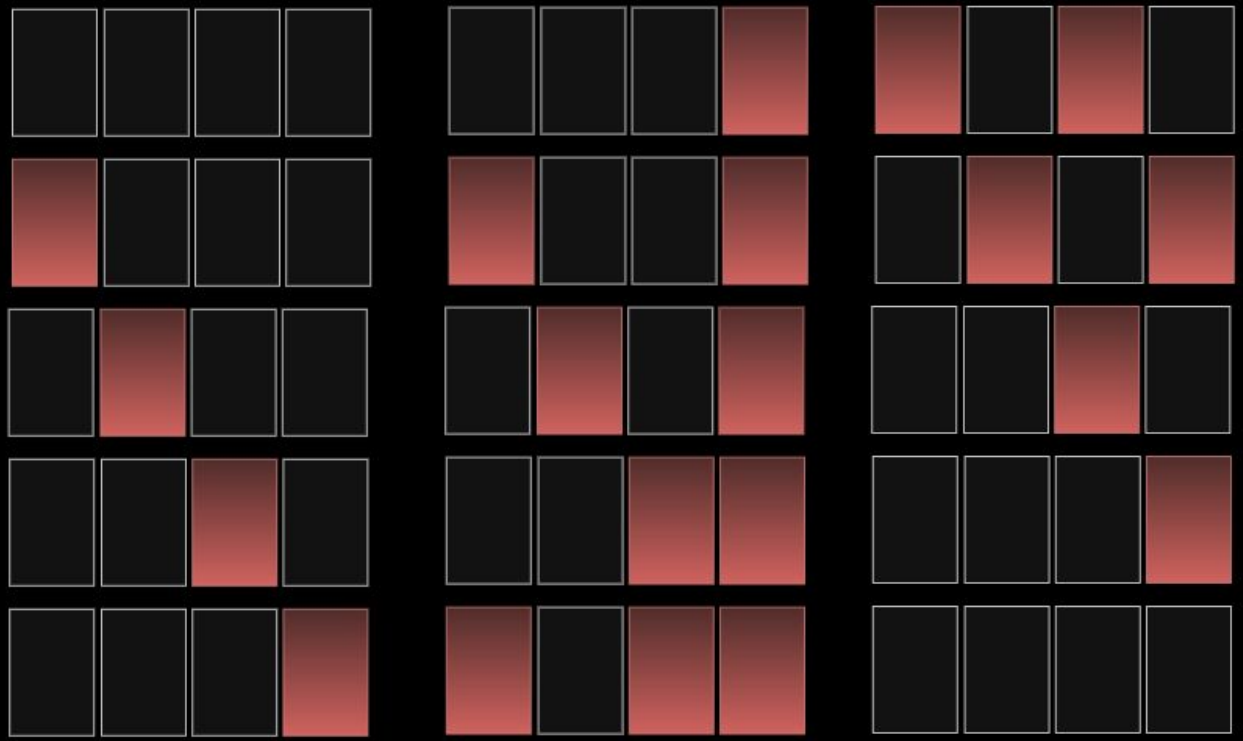
Event Driven Register



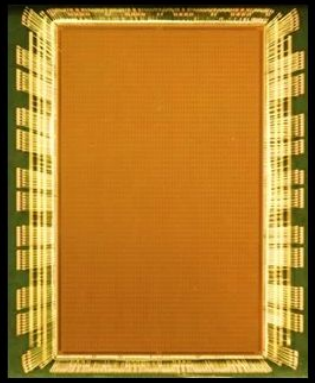
The Asynchronous Pipeline



The Asynchronous Pipeline



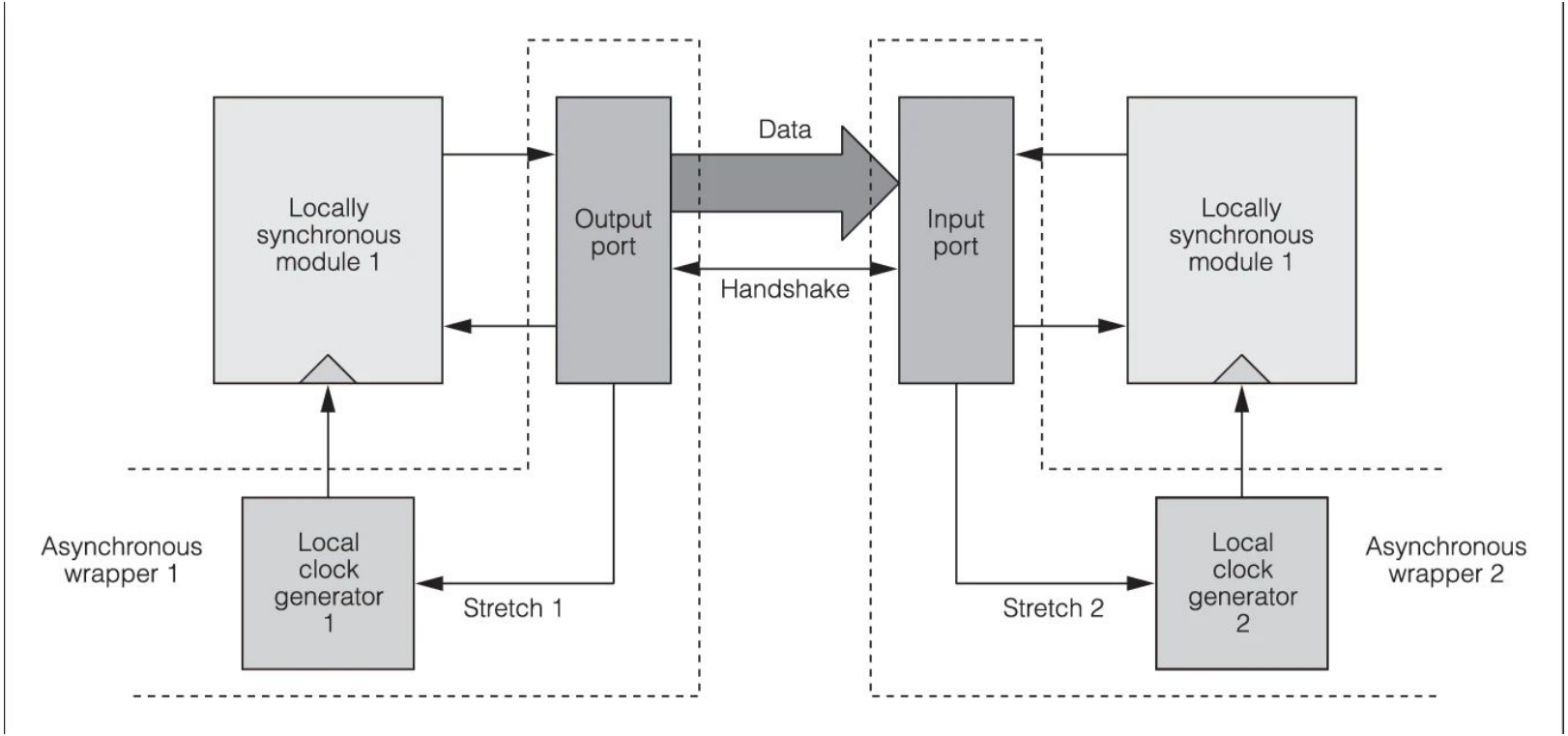
The Asynchronous Pipeline



TrueNorth

1 M Neurons
256 M Synapses
5.4 B Transistors
Realtime
73 mW

The Asynchronous Pipeline



What's Next?

Join our discord server! We have a async-circuits channel where you can find the slides, recording (once uploaded), and a paper bundle of relevant papers to read about the topic! Feel free to discuss what you thought about the event there as well.

Stay connected with us on our website: https://ieeeuoft-asic.github.io